associated overhead data to the addressed at least one of the memory array cell groups, and

in response to receipt from the host processor of a command to read user data from said at least one mass memory storage block address, reading at least one sector of said user data and associated overhead data from the addressed at least one of the memory array cell groups.

64. The method according to claim 63, wherein, in response to receipt from the host processor of a command to write user data, first processing the overhead data associated with the user data stored in the addressed at least one of the groups of array cells.

65. The method according to claim 63, wherein, in response to receipt from the host processor of a command to read user data, first processing the overhead data associated with the user data stored in the addressed at least one of the groups of array cells.

66. The method according to any one of claims 63-65, wherein the overhead data stored within the addressed at least one of the groups of array cells includes the address of said at least one group.

67. The method according to claim 63, additionally comprising:

detecting a predefined condition when individual ones of the groups of array cells become unusable and linking the addresses of such unusable groups with addresses of other groups of array cells that are useable, and

wherein addressing said at least one of the groups of array cells includes referring to the linked address of another group that is usable and then mapping said at least one mass memory storage block address into such another group.

68. The method according to claim 67, wherein detecting of the predefined condition includes detecting when individual groups of array cells have become defective.

69. The method according to claim 68, wherein detecting when individual groups of array cells become defective includes

36

determining when a number of individual defective memory cells within a group exceed a given number.

10. The method according to claim 1, wherein linking the address of unusable groups of array cells with groups that are useable includes maintaining a list that links such unusable groups with addresses of corresponding ones of other groups that are useable, and wherein addressing a usable group includes referring to the list to translate the address of the unusable group into an address of a usable group.

11. The method according to claim 1, wherein linking the address of such unusable groups includes storing within individual ones of the defective groups addresses of corresponding useable groups, and wherein addressing a usable group corresponding to an unusable group includes referring to the useable group address stored in the unusable group.

12. The method according to any one of claims 1-3 or ~~63-65 and 67-71~~, wherein the mass memory storage block address is a magnetic disk sector.

13. The method according to claim 12, wherein the mass memory storage block address includes designation of a magnetic disk drive head, cylinder and sector.

~~14. The method according to any one of claims 1-3 or 63-65 and 67-71, wherein the amount of user data stored in individual ones of the groups of array cells is substantially the same as the amount of user data contained in individual ones of said mass memory storage blocks.~~

15. The method according to claim 14, wherein said amount of user data is substantially 512 bytes.

16. The method according to any one of claims 1-3 or 63-65 and 67-71, wherein said bulk storage memory is implemented in a single package.

~~17. The method according to claim 16, wherein said bulk storage memory is provided within a card that is removably connectable to the computer system through an electrical connector.~~

18. The method according to any one of claims 1-3 or 63-65 and 67-71, further comprising erasing data from a selected at least one of the individual groups of array cells by simultaneously applying

an erase voltage to all of the cells within said selected at least one group, thereby to simultaneously erase any user data and associated overhead data contained in said at least one group of cells.

79. The method according to claim 78, wherein the memory array cells individually include erase gates, and the erase voltage is simultaneously applied to the erase gates of said selected at least one group of array cells.

~~80. The method according to claim 74, wherein said bulk storage memory is provided within a single card that is removably connectable to the computer system through an electrical connector.~~

81. The method according to claim 74, further comprising erasing data from a selected at least one of the individual groups of array cells by simultaneously applying an erase voltage to all of the cells within said selected at least one group, thereby to simultaneously erase any user data and associated overhead data contained in said at least one group of cells.

82. A bulk storage memory system that is connectable to a host computer system, said memory system comprising:

an array of non-volatile floating gate memory cells arranged to store in designated locations thereof a plurality of blocks of a given amount of user data and associated units of overhead data, and

a controller connectable to said computer system for controlling operation of the array, said controller including:

an addressing circuit responsive to receipt of a mass memory storage block address from the host computer system to address a corresponding block of user data and its associated unit of overhead data,

a reading circuit responsive to the addressing circuit to read a unit of overhead data associated with the addressed block of user data, and

a reading circuit responsive to the addressing circuit and the read unit of overhead data to execute an instruction from the host computer system to perform a designated one of reading user data from, or writing user data to, the addressed user data block.

83. The memory according to claim 82 additionally comprising a list of any unusable ones of said designated locations to link said unusable locations with others of said locations that are usable, and wherein said addressing circuit includes a circuit to access linked others of said locations in place of said unusable locations.

84. The memory according to claim 83 wherein the list of unusable locations includes a list maintained within the bulk storage memory outside of locations of the memory array designated to store blocks of user data and associated units of overhead data.

85. The memory according to claim 83 wherein the list of unusable locations includes a list stored as part of units of overhead data associated with unusable locations of the memory array.

86. The memory according to any one of claims 83-85 wherein the list of any unusable locations includes inoperable or defective locations.

87. The memory according to any one of claims 83-85 wherein the list of any unusable locations includes locations that contain a number of defective cells in excess of a preset number.

88. The memory according to any one of claims 82-85 wherein said given amount of user data is substantially 512 bytes.

89. The memory according to any one of claims 82-85 wherein said mass memory storage block address is a magnetic disk sector address.

90. The memory according to claim 89 wherein said magnetic disk sector address includes a head, cylinder and sector.

91. The memory according to any one of claims 82-85, wherein said bulk storage memory is implemented in a single package.

92. The memory according to claim 91, wherein said bulk storage memory is provided within a card that is removably connectable to the computer system through an electrical connector.

93. The memory according to any one of claims 82-85, wherein individual blocks of user data and corresponding units of overhead data are stored together within individual ones of a plurality of locations of the memory cell array.